

## Article Abstract

Title:	Multi-level sequential circuit partitioning for test vector generation for low power test in VLSI
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Abstract:	Sequential graph partitioning algorithms have been developed to fulfill the requirements of emerging multi-phase problems in circuit testing models. In this paper, we present a multi-level graph partitioning algorithm for circuit partitioning, which will minimize the number of test vectors during a low power test in VLSI circuits. By reducing the number of test vectors, we can reduce the energy consumption during the test. Our experimental results with ISCAS bench mark circuits have shown that the power can be reduced up to 55%.
Keywords:	Graph partitioning, Circuit partitioning, BIST, Automatic test pattern generation, Low power test.